IN THE CLAIMS:

1. (Currently Amended) A diagnostic compiler for use with a pipeline analog-to-digital converter (ADC) having code sequences corresponding to stages thereof, comprising:

a transition locator configured to determine transition locations for said code sequences based on a design of said pipeline ADC; and

a characteristics indicator coupled to said transition locator and configured to provide at least one characteristic of said pipeline ADC based on said transition locations.

2. (Original) The diagnostic compiler as recited in Claim 1 wherein said determination of transition locations is configured to employ a mathematical function based on said stages.

3. (Original) The diagnostic compiler as recited in Claim 2 wherein said mathematical function is configured to employ an attribute selected from the group consisting of:

orthogonality, and

bi-state functionality.

4. (Original) The diagnostic compiler as recited in Claim 1 wherein said at least one characteristic is configured to represent a stage mismatch error of said ADC.

5. (Original) The diagnostic compiler as recited in Claim 4 wherein said stage mismatch error is configured to contain an attribute selected from the group consisting of:

capacitive mismatch,

resistive mismatch, and

comparative mismatch.

6. (Original) The diagnostic compiler as recited in Claim 1 wherein said at least one characteristic is configured to represent an offset error of said ADC.

7. (Original) The diagnostic compiler as recited in Claim 1 wherein said at least one characteristic is configured to represent a superposition error of said ADC.

8. (Currently Amended) A method of compiling for use with a pipeline analog-to-digital converter (ADC) having code sequences corresponding to stages thereof, comprising:

determining transition locations for said code sequences based on a design of said pipeline ADC; and

providing at least one characteristic of said pipeline ADC based on said transition locations.

9. (Original) The method as recited in Claim 8 wherein said determining transition locations employs a mathematical function based on said stages.

10. (Original) The method as recited in Claim 9 wherein said mathematical function employs an attribute selected from the group consisting of:

orthogonality, and

bi-state functionality.

11. (Original) The method as recited in Claim 8 wherein said providing at least one

characteristic represents a stage mismatch error of said ADC.

12. (Original) The method as recited in Claim 11 wherein said stage mismatch error contains an attribute selected from the group consisting of:

capacitive mismatch,

resistive mismatch, and

comparative mismatch.

13. (Original) The method as recited in Claim 8 wherein said providing at least one characteristic represents an offset error of said ADC.

14. (Original) The method as recited in Claim 8 wherein said providing at least one characteristic represents a superposition error of said ADC.

15. (Currently Amended) A test system, comprising:

a data processing unit that has a device testing interface;

a pipeline analog-to-digital converter (ADC) that is coupled to said device testing interface and has code sequences corresponding to stages thereof; and

a diagnostic compiler that is coupled to said pipeline ADC, including:

a transition locator that determines transition locations for said code sequences based on a design of said pipeline ADC; and

a characteristics indicator, coupled to said transition locator, that provides at least one characteristic of said pipeline ADC based on said transition locations.

16. (Original) The system as recited in Claim 15 wherein said determination of transition locations employs a mathematical function based on said stages.

17. (Original) The system as recited in Claim 16 wherein said mathematical function employs an attribute selected from the group consisting of:

orthogonality, and

bi-state functionality.

18. (Original) The system as recited in Claim 15 wherein said at least one characteristic represents a stage mismatch error of said ADC.

19. (Original) The system as recited in Claim 18 wherein said stage mismatch error contains an attribute selected from the group consisting of:

capacitive mismatch,

resistive mismatch, and

comparative mismatch.

20. (Original) The system as recited in Claim 15 wherein said at least one characteristic represents an offset error of said ADC.

21. (Original) The system as recited in Claim 15 wherein said at least one characteristic represents a superposition error of said ADC.